NON-VOLATILE SEMICONDUCTOR LATCH USING HOT-ELECTRON INJECTION DEVICES

Introduction

This invention concerns semiconductor latches capable of memorizing the programmed information even after their power supply has been removed. The invention was applied to a 0.6μm BiCMOS EPROM process but it is applicable in any other process having hot electron injection devices like EPROM, Flash EEPROM, etc.

Background

Several types of non-volatile semiconductor latches are known in the prior art. They use different kind of non-volatile memory elements like fuses, MNOS transistors, EPROM transistors, standard EEPROM transistors, Flash EEPROM transistors, etc. Normally the transistor memory elements need a programming voltage relatively higher than the normal power supply. For many technological processes this means that almost all transistors in the non-volatile latch have to be made by high-voltage (HV) transistors instead of normal low-voltage (LV) transistors. As a result, the non-volatile latch area, a critical parameter, may increase a lot in size.

Additional problem exists in the non-volatile latches using hot-electron injection devices like EPROM and Flash EEPROM transistors. Normally they need a large current for programming, for example 0.5 to 1.0mA/bit, in contrast to the standard EEPROM transistors using Fowler-Nordheim tunnel injection which takes, for example about 10pA/bit. So, a disposal of hot-electron injection devices in a non-volatile latch, for example in the way described in **GB-A 2 054 303** (Hughes Microelectronics), will require a large programming current flowing though the data line, respectively very large transistors along the drain

programming path of the hot-electron injection devices. This will cause an additional increase of the non-volatile latch area and the area of its periphery.

These problems are solved by **US-A 5,428,571** (Atsumi et al.), splitting the hot-electron injection device into two parts: A reading transistor and a writing transistor with a common floating gate. But a limitation of this design solution is the use of depletion transistors that are not available in each process. Another limitation of this approach is that the threshold voltage of the depletion-type reading transistor has to be increased to positive values for avoiding a static current in the non-volatile latch. This leads to strong requirements to the latch programming and decreases the data retention time of the latch.

Summary

An **object of the invention** is to provide a non-volatile latch using hot-electron injection devices. The high voltage for programming has to be applied on a largely reduced number of elements for decreasing the total latch area.

Another object of the invention is to provide a reliable work and no static current even at a weak programming of the hot-electron injection devices.

A further object of the invention is the use of enhancement transistors only, so that it is applicable to any non-volatile process.

For achieving the above objects, a bi-stable non-volatile semiconductor latch is proposed (claim 1). It has got a pair of cross-coupled branches, each branch including a complementary driver and a load connected between a drain line and a source line and a non-volatile memory cell having a program transistor and a read transistor. Each driver includes a read transistor. The driver and the load of a branch are connected in series at a

respective output node. The read transistor and the program transistor in a branch have got a common floating gate and separate control gates. The control gate of the program transistor is connected to a program voltage and its drain is connected to a respective input node. The control gate of the read transistor in a branch is connected to the output node of the other branch.

Embodiments enhance the invention's understanding.

Introduction to the Drawings

Fig. 1 represents a schematics circuit of an embodiment of the invention.

Fig. 2 shows a layout example of a read transistor and a program transistor with common floating gate in 0.6µm one-poly-level BiCMOS EPROM process.

Fig. 3 represents a further embodiment of the invention.

Detailed Description of embodiments

The first embodiment of the invention is shown in **Figure 1**. The non-volatile latch consists of two branches, I and II. Branch I has transistors T1, T3, T5 and T7. Branch II has transistors T2, T4, T6 and T8. Transistors T1 and T2 are LV NMOS transistors. Transistors T3 and T4 are LV PMOS transistors and represent the load of the respective branch. The source of transistors T3 and T4 is connected to a drain line 11 which can be the common power supply line. The drain of transistor T3 is connected to an output Q and the drain of transistor T4 is connected to an inverted output $\overline{Q}$.

The read transistor T5 and the program transistor T7 are parts of a non-volatile memory cell with a common floating gate 13. The read transistor T5 is connected in series with transistor T1 between the output Q and a source line 12. Transistors T1 and T5 represent the driver of branch I.

The read transistor T6 and the program transistor T8 are parts of another non-volatile memory cell with a common floating gate 14. The read transistor T6 is connected in series with transistor T2 between the inverted output $\overline{Q}$ and the source line 12. Transistors T2 and T6 represent the driver of branch II.

The control gate 15 of the read transistor T5 and the gates of transistors T1 and T3 are connected to the inverted output $\overline{Q}$. The control gate 16 of the read transistor T6 and the gates of transistors T2 and T4 are connected to the output Q. These two cross-coupled connections make the non-volatile latch bi-stable.

The source line 12 can be connected to the common ground line in static mode but it is disconnected (made floating) in program mode.

The drain of the program transistor T7 is connected to a data input D. The drain of the program transistor T8 is connected to an inverted data input $\overline{D}$. Both data inputs D and $\overline{D}$ are set to ground in static mode. In program mode one of them is raised to a middle range voltage, for example 7.5V for a 0.6µm BiCMOS EPROM process, enough to generate hot electrons at the respective drain.

The source of the program transistors T7 and T8 is connected to ground and their respective control gates 17 and 18 are connected to a program voltage input 19. The program voltage is set to the common power supply voltage in static mode, for example 5V. In program mode it is raised to a higher value, for example 12.5V for the 0.6µm BiCMOS EPROM process, so that this voltage is enough to inject hot electrons into the respective floating gate.

It is obvious that high programming voltage is applied only on the control gates 17 and 18 of the program transistors T7 and T8. So, all other transistors in the present non-volatile latch, including the input driving circuitry not shown in Fig.1, can be standard LV MOS transistors with minimal dimensions for a layout area decrease.

Also the program voltage input can be common for a plurality of such non-volatile latches, so that HV MOS transistors can be placed only in a reduced HV switching peripheral circuitry. In

this way an additional decrease of the total layout area can be achieved.

The programming of the non-volatile latch can be done by applying simultaneously pulses on the program voltage input 19 and a selected data input, for example D. At these conditions the floating gate 13 traps charges by hot electron injection. The threshold voltage of the read transistor T5 increases in respect to that of the read transistor T6.

As both branches of the non-volatile latch are made symmetrical even a small difference between the threshold voltages of the read transistors T5 and T6 will be enough to turn the non-volatile latch in the correct programmed state after each subsequent turning off and on of the power supply. It is obvious for the skilled in the art that the load at the outputs Q and $\overline{Q}$ has to be equal for a full symmetry.

In case of a weak programming the voltage on the floating gates 13 and 14 can be higher than the threshold voltages of the read transistors T5 and T6 during power on. Then the enhancement NMOS transistors T1 and T2 included in the drivers of the bi-stable latch provide a zero current consumption in static mode.

Figure 2 represents the layout view of the memory cell including the read transistor T5 and the program transistor T7 in 0.6µm one-poly-level BiCMOS EPROM process. The floating gate 13 is made by polysilicon. The other process layers shown in Fig. 2 are: active area 43, collector implant (buried n+ layer) 41, and contact hole layer 44. The transistor terminals are named in the same way like in Fig. 1.

As it can be seen in Fig. 2 the coupling ratio of the program transistor T7 is done bigger than that of the read transistor T5. This is needed for improving the hot-electron injection efficiency since the control gate 15 is held at a lower voltage than the control gate 17 in program mode.

It is obvious for the skilled in the art that the memory cell shown in Fig. 2 can be done in many other different ways depending on the used non-volatile process. For example, a stacked polysilicon gate can be used for manufacturing (second polysilicon layer for the control gates).

Figure 3 shows a more detailed embodiment of the invention. The drain line is substituted by the common power supply line. The source line 12 is connected to ground through the NMOS transistor T9 in static mode ($\overline{PGM}$ = '1') whereas in program mode transistor T9 is turned off ($\overline{PGM}$ = '0') and the source line 12 is floating. The PMOS transistors T11 and T12 are off in static mode bit in program mode they pull up the outputs Q and $\overline{Q}$ to the common power supply. In this way the non-volatile latch easily turns in the correct programmed state after the programming pulse end.

All transistors in Fig. 3, including the input driving circuitry not shown in the picture, are enhancement type transistors, so the implementation of the invention is easy in other non-volatile processes.

Prior Art review.

In **GB-A 2 054 303** (see initial section) the WHOLE non-volatile element, IGFET Q3, is included in the complementary driver (Q3, Q5 - Fig. 1) or in the complementary load (Q1, Q3 - Fig. 5). The same applies for the IGFET Q4 in the other branch. In the embodiments the non-volatile element (cell) is split in two parts - a read transistor and a program transistor. Only the read transistor T5 is included in the complementary driver (T1, T5 - Fig. 1). The same applies for T6 in the other branch. The other part of the non-volatile element (cell) in the embodiments, the program transistor T7, is not included in the complementary driver (compare to GB 2 054 303, there CLAIMS, lines 46 to 49). The same applies for T8 in the other branch.

In same GB-A 2 054 303 the input data for programming the non-volatile (NV) latch are provided through a WRITE transistor Q9 (and Q11 in Fig. 3 and 4) and applied to the respective nodes X (and Y in Fig. 3 and 4). In the embodiments the input data for programming of the NV latch are applied on the drain of the program transistors T7 and T8, therefore the input data are decoupled from the respective output nodes Q and Q| (quer).

In same GB-A 2 054 303 the NV-latch is programmed by applying a high voltage (HV) on the control gate of the transistors Q3 or Q4 (See Fig. 1 and 5), i.e. on the respective nodes X or Y. (See also rows 56 to 61 of the patent background.) It means that all transistors (except Q10 and Q12) of this latch may be put under HV during programming. In the embodiments the NV latch is programmed by applying HV only on the node 19 (see Fig.1 and 3). Therefore the HV is decoupled from the respective output nodes Q and Q| and only the gates of the program transistors T7 and T8 are put under HV during programming.

In same GB-A 2 054 303 the NV-latch needs buffers (Q7, Q8) and/or READ transistors (Q10, Q12) between the respective nodes X and Y from one side and the DATA line from other side. (See also rows 53 to 56 of the claims). In the embodiments the NV latch nodes Q and Q| can be used directly as respective NV latch outputs.

A Comparison between the inventive embodiments and **US-A 4,399,522** is: There the non-volatile element 12 (Fig. 1) used in the RAM cell is ONE transistor with common drain 34, common source 36, common floating gate 24 and two control gates (30 and 46). The same applies for the other non-volatile element 14. Also in the inventive embodiments "a said transistor (i.e. one transistor) having first and second control gates, a floating gate". In the embodiments the non-volatile element (cell) used in the NV latch consists in fact of TWO transistors (T5 and T7) with only common the floating gate 13. In could be seen in all Figures that the drain (Q), the source (21) and the control gate (15) of T5 are different from the drain (D), the

source (ground) and the control gate (17) of T7. The same for the non-volatile element (cell) used in the other branch – it also consists of TWO separate transistors T6 and T8 with only common the floating gate 14.

In US-A 5,428,571 the reading transistor (T4, all Figures) is depletion type (see also claims 1 and 12) whereas the writing transistor (T3, all Figures) is enhancement type. In the embodiments both the read transistor (T5, T6) and the program transistor (T7, T8) are enhancement type.

In same US-A 5,428,571 the NV latch needs additional protection means like the depletion transistor T2 (see also claims 1 and 12). In the embodiments the NV latch does not need such protection means. There is no depletion transistor at all in the proposed NV latch.

In same US-A 5,428,571 the reading and the writing transistors have got a common control gate connected to Vpp/Vss (Fig. 1, 2, 4 and 5). Only in Fig. 3 a variant with two control gates is shown but the control gate of the reading transistor T4 is connected to ground (Vss). In the embodiments the non-volatile cell (T5, T7) has got two separate control gates. The control gate of the read transistor T5 is connected to the respective output node Q|. The same for the other memory cell (T6, T8).

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